TITLE **800G OSFP SR8 Transceiver**	**DOC No. RFD-20240112002-002**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
	DATE：2024.01.12	**CLASSIFICATION：CONFIDENTIAL**

1.Introduction

800G OSFP SR8 is a cost effective module with high performance, which is optimized for datacenter, supporting data-rate of 8 × 53.125 GBd PAM4. Its transmission distance is up to 100m on OM4 MMF. The module mainly consists of two parts: the transmitter part and the receiver part. The transmitter part consists of 850nm VCSEL array and driver. The receiver part consists of trans

-impedance amplifier (TIA) and PIN photodiode array. The high-speed electrical interface is based on low-voltage logic, with nominal 100 ohm differential impedance, AC coupled in the module. Users can access a series of registers in transceiver to access monitoring and configuration data through two wire serial interface. This interface uses a single address, A0h, with a memory map divided into a lower and upper area. Basic digital diagnostic (DD) data is held in the lower area while specific data is held in a series of tables in the high memory area.

2.Features and Applications Compliance

- 53.125 GBd PAM4 ×8 channel 800G AUI-8 C2M Electrical interface
- 53.125 GBd PAM4 ×8 channel 800G-SR8 Optical interface
- 850nm VCSEL and PIN receiver
- OSFP MSA package with MPO-16 APC
- Very low EMI and excellent ESD protection
- +3.3V power supply
- Power consumption less than 14W
- Operating case temperature: 0~70°C
- IIC rate up to 1MHz
- Up to 100m transmission distance on OM4/OM5 MMF

TITLE 800G OSFP SR8 Transceiver	DOC No. RFD-20240112002-002	
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2024.01.12	CLASSIFICATION：CONFIDENTIAL

3. Applications and Compliance

- 800G Ethernet
- Datacenter switch
- Compliant with OSFP MSA
- Compliant with IEEE 802.3db
- Compliant with IEEE 802.3ck
- Compliant with CMIS Rev5.2
- Compliant with OIF-CEI-05.0
- Compatible with InfiniBand
- Compliant with RoHS6

4.PRODUCT DESCRIPTION

4.1PRODUCT NAME AND SERIES NUMBER(S)

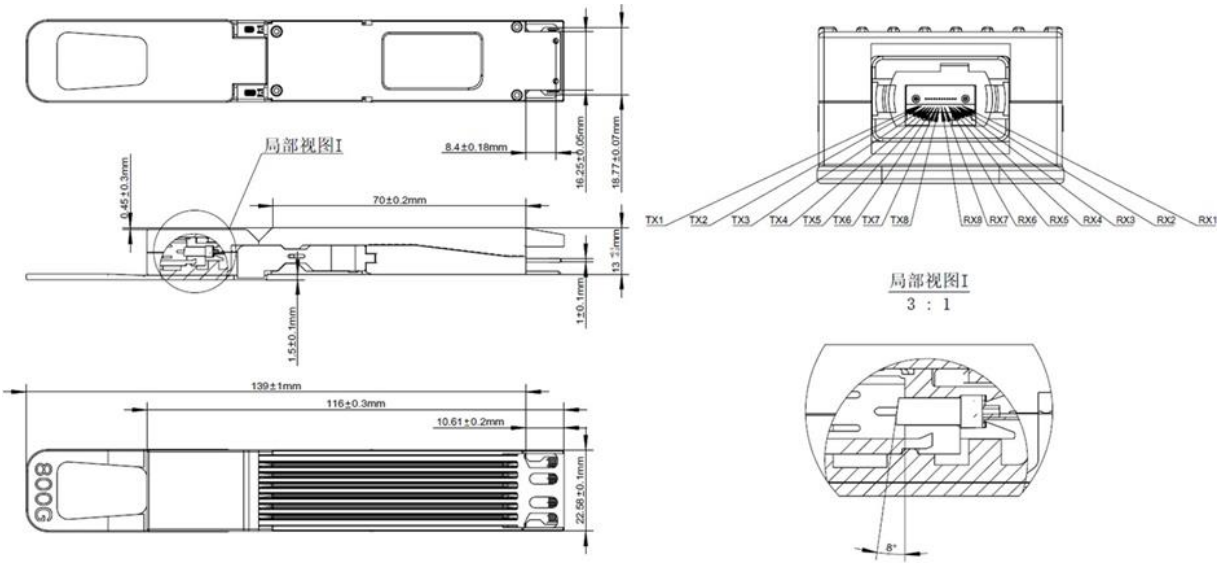
800G OSFP SR8 Transceiver

Part Number	Data Rate	Wavelength (nm)	Distance	Power (dBm)	Sen. (dBm)	Connector	Temp.
TNP69008KUCAS1-K	800G	850	100m (om4/om5)	-4.6~4	-4.4	MPO-16	C

TITLE 800G OSFP SR8 Transceiver	DOC No. RFD-20240112002-002	
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2024.01.12	CLASSIFICATION：CONFIDENTIAL

4.2DIMENSIONS, MATERIALS, PLATINGS AND MARKING

See the package outline for details.



Mechanical Package Outline (All dimensions in mm)

5.Product Specification

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	Tstg	-40		85	ºC	
Operating Relative Humidity	RH	5		85	%	Note1
Supply Voltage	VCC	-0.5		3.6	V	
Receiver Damage Threshold, each lane	PIN	5			dBm	

Note:

1. Non-condensing

TITLE 800G OSFP SR8 Transceiver	DOC No. RFD-20240112002-002	
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2024.01.12	CLASSIFICATION：CONFIDENTIAL

5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Case temperature	Tcase	0		70	℃	
Supply Voltage	VCC	3.135	3.3	3.465	V	
Supply Current	ICC			4466	mA	
Module Power Dissipation	P			14	W	

5.3 General Optical & Electrical Characteristics of Transmitter

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Data Rate per channel（PAM4）	DR		53.125		GBd	
Frequency tracking	Ft	-100		100	ppm	
Center Wavelength	λ_C		850		nm	
RMS Spectral Width				0.6	nm	Note1
Laser Off Power	Poff			-30	dBm	
Average Optical Power	Pavg	-4.6		4	dBm	
Extinction Ratio	ER	2.5			dB	
Transmitter and dispersion eye closure	TDECQ			4.4	dB	
Outer Optical Modulation Amplitude	OMAouter	-2.6		3.5		Note2
Encircled flux, each lane	dB	≥ 86% @ 19 μm ≤ 30% @ 4.5 μm				Note3
Optical Return Loss Tolerance				14	dB	

Notes:

1.RMS spectral width is the standard deviation of the spectrum.

2.if max(TECQ,TDECQ)≤1.8dB, the OMA (min)=-2.6 ； if 1.8 ＜ max(TECQ,TDECQ)≤4.4dB, the OMA (min)= -4.4+max(TECQ,TDECQ)；

3.If measured into type A1a.2, type A1a.3 or type A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4.

TITLE 800G OSFP SR8 Transceiver	DOC No. RFD-20240112002-002	
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2024.01.12	CLASSIFICATION：CONFIDENTIAL

5.4 General Optical & Electrical Characteristics of Receiver

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data Rate per channel（PAM4）	DR		53.125		GBd	
Frequency tracking	Ft	-100		100	ppm	
Center Wavelength	λr		850		nm	
Average receive power		-6.4		4	dBm	Note1
Receiver Reflectance				-15	dB	
Receiver sensitivity(OMAouter)				Max(-4.6,-6.4+TECQ)		Note2
Differential Data Output Voltage Peak to Peak Swing，Short mode	Vopp			600	mV	
Differential Data Output Voltage Peak to Peak Swing，Long mode	Vopp			845	mV	
Eye height	EH	15			mV	
Vertical eye closure	Vec			12	dB	
Differential output Impedance	Zos	90	100	110	ohm	
Common-Mode to differential-mode return loss	RLdc	Note2				
Transition Time, 20 to 80%	Tr, Tf	8.5			ps	

Notes:

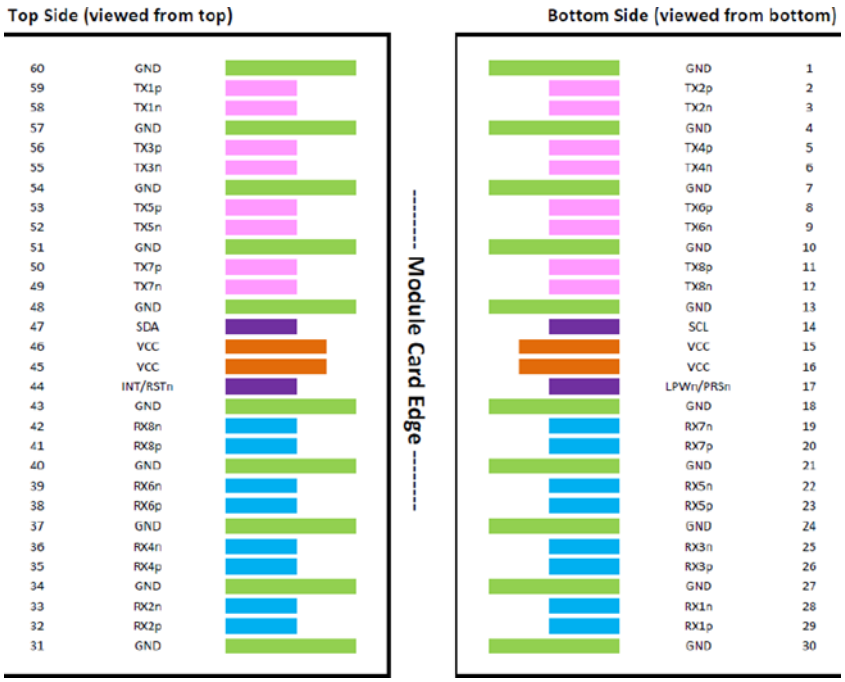
1.Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

2.If TECQ≤1.8dB, the OMA (min)=-4.6;Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB.

TITLE 800G OSFP SR8 Transceiver	DOC No. RFD-20240112002-002	
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2024.01.12	CLASSIFICATION：CONFIDENTIAL

$$RLdc(f) \geq \begin{cases} 25 - 22(f/53.125) & 0.05 \leq f \leq 26.56 \\ 19 - 10(f/53.125) & 26.56 < f \leq 50 \end{cases}$$

6.Pin Assignments



QSFP Pad Function Definition

Electrical Pin Definition(OSFP)

Pad	Logic	Symbol	Name/Description	Plug Sequence	Note
1		GND	Ground	1	
2	CML-I	TX2p	Transmitter Non-Inverted Data Output	3	
3	CML-I	TX2n	Transmitter Inverted Data Output	3	
4		GND	Ground	1	

TITLE **800G OSFP SR8 Transceiver**	**DOC No. RFD-20240112002-002**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
	DATE：2024.01.12	**CLASSIFICATION：CONFIDENTIAL**

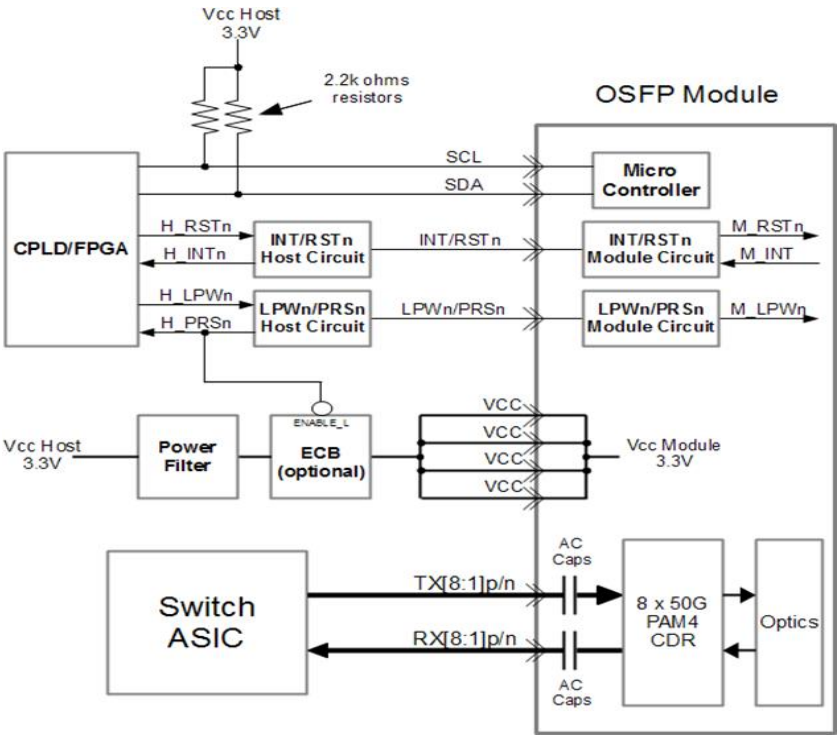
5	CML-I	TX4p	Transmitter Non-Inverted Data Output	3	
6	CML-I	TX4n	Transmitter Inverted Data Output	3	
7		GND	Ground	1	
8	CML-I	TX6p	Transmitter Non-Inverted Data Output	3	
9	CML-I	TX6n	Transmitter Inverted Data Output	3	
10		GND	Ground	1	
11	CML-I	TX8p	Transmitter Non-Inverted Data Output	3	
12	CML-I	TX8n	Transmitter Inverted Data Output	3	
13		GND	Ground	1	
14	LVCMOS-I/O	SCL	2-wire Serial interface clock	3	
15		VCC	+3.3V Power	2	
16		VCC	+3.3V Power	2	
17	Multi-Level	LPWn/PRSn	Low-Power Mode / Module Present	3	
18		GND	Ground	1	
19	CML-O	RX7n	Receiver Inverted Data Input	3	
20	CML-O	RX7p	Receiver Non-Inverted Data Input	3	
21		GND	Ground	1	
22	CML-O	RX5n	Receiver Inverted Data Input	3	
23	CML-O	RX5p	Receiver Non-Inverted Data Input	3	
24		GND	Ground	1	
25	CML-O	RX3n	Receiver Inverted Data Input	3	
26	CML-O	RX3p	Receiver Non-Inverted Data Input	3	
27		GND	Ground	1	
28	CML-O	RX1n	Receiver Inverted Data Input	3	
29	CML-O	RX1p	Receiver Non-Inverted Data Input	3	
30		GND	Ground	1	
31		GND	Ground	1	

TITLE **800G OSFP SR8 Transceiver**	**DOC No. RFD-20240112002-002**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
	DATE：2024.01.12	**CLASSIFICATION：CONFIDENTIAL**

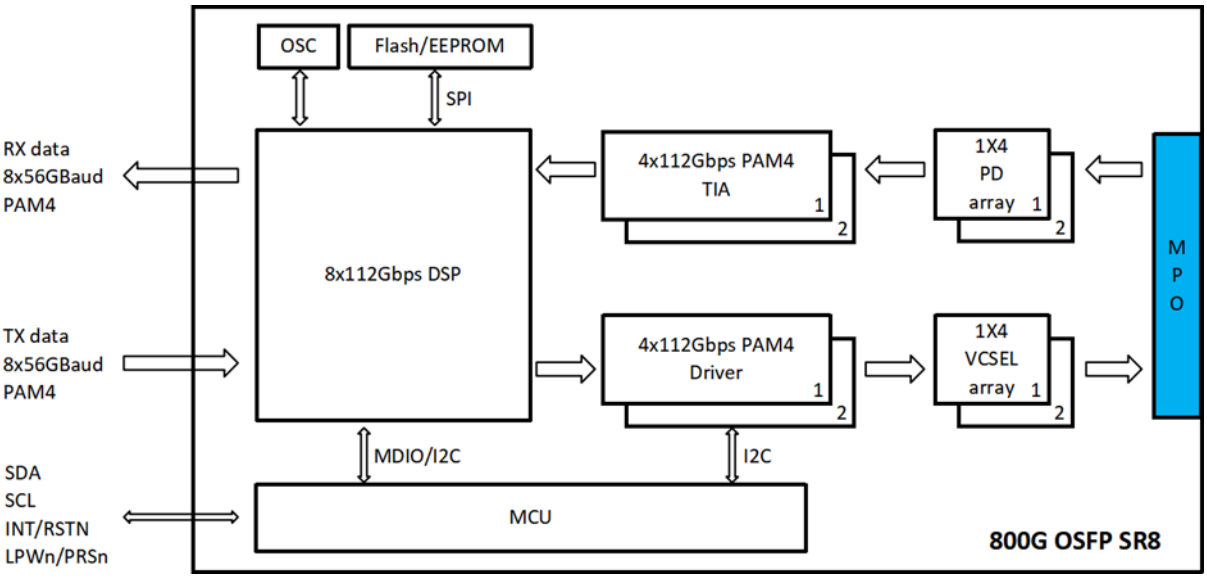
32	CML-I	RX2p	Receiver Non-Inverted Data Input	3	
33	CML-I	RX2n	Receiver Inverted Data Input	3	
34		GND	Ground	1	
35	CML-I	RX4p	Receiver Non-Inverted Data Input	3	
36	CML-I	RX4n	Receiver Inverted Data Input	3	
37		GND	Ground	1	
38	CML-I	RX6p	Receiver Non-Inverted Data Input	3	
39	CML-I	RX6n	Receiver Inverted Data Input	3	
40		GND	Ground	1	
41	CML-I	RX8p	Receiver Non-Inverted Data Input	3	
42	CML-I	RX8n	Receiver Inverted Data Input	3	
43		GND	Ground	1	
44	Multi-Level	INT/RSTn	Module Interrupt / Module Reset	3	
45		VCC	+3.3V Power	2	
46		VCC	+3.3V Power	2	
47	LVCMOS-I/O	SDA	2 wire serial interface data	3	
48		GND	Ground	1	
49	CML-I	TX7n	Transmitter Inverted Data Output	3	
50	CML-I	TX7p	Transmitter Non-Inverted Data Output	3	
51		GND	Ground	1	
52	CML-I	TX5n	Transmitter Inverted Data Output	3	
53	CML-I	TX5p	Transmitter Non-Inverted Data Output	3	
54		GND	Ground	1	
55	CML-I	TX3n	Transmitter Inverted Data Output	3	
56	CML-I	TX3p	Transmitter Non-Inverted Data Output	3	
57		GND	Ground	1	
58	CML-I	TX1n	Transmitter Inverted Data Output	3	
59	CML-I	TX1p	Transmitter Non-Inverted Data Output	3	
60		GND	Ground	1	

TITLE 800G OSFP SR8 Transceiver	DOC No. RFD-20240112002-002	
	REVISION : 01	AUTHORIZED BY : Andy Yang
	DATE : 2024.01.12	CLASSIFICATION : CONFIDENTIAL

Recommended Power Supply Filter



Block Diagram of Transceiver



TITLE 800G OSFP SR8 Transceiver	DOC No. RFD-20240112002-002	
	REVISION：01	AUTHORIZED BY：Andy Yang
	DATE：2024.01.12	CLASSIFICATION：CONFIDENTIAL

Digital Diagnostic Functions and Control and Status I/O Timing Characteristics

a. Diagnostic Functions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Temperature monitor absolute error	DMI_Temp	-3		3	℃	
Tx power monitor absolute error	DMI_TX	-3		3	dB	
Rx power monitor absolute error	DMI_RX	-3		3	dB	
Supply voltage monitor absolute error	DMI_VCC	-5		5	%	
Bias current monitor absolute error	DMI_Ibias	-10		10	%	

b. Control and Status I/O Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Max Time to reach manageability in ModuleLowPwr	tMgmtInit			2000	ms	Note1
Reset Assert Duration	t_reset_init	10			us	Note2
Interrupt Assert Time	ton_Int			200	ms	Note3
Interrupt Deassert Time	toff_Int			0.5	ms	Note4
Rx LOS Interrupt Assert Time	ton_los			100	ms	Note5
Tx Failure Interrupt Assert Time	ton_Txfail			200	ms	Note6
Flag Assert Time	ton_flag			200	ms	Note7
Mask Assert Time	ton_mask			100	ms	Note8
Mask Deassert Time	toff_mask			100	ms	Note9
Tx Output Disable Latency	ton_txdis			100	ms	Note10
Tx Output UnDisable Latency	toff_txdis			400	ms	Note11
Rx Output Disable Assert Time	ton_rxdis			100	ms	Note12
Rx Output Disable Deassert Time	toff_rxdis			100	ms	Note13
Auto Squelch Disable Assert Time	ton_sqdis			100	ms	Note14

TITLE **800G OSFP SR8 Transceiver**	**DOC No. RFD-20240112002-002**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
	DATE：2024.01.12	**CLASSIFICATION：CONFIDENTIAL**

Auto Squelch Disable Deassert Time	toff_sqdis			100	ms	Note15
Rx Auto Squelch Reaction Latency	ton_Rxsq			15	ms	Note16
Tx Auto Squelch Reaction Latency	ton_Txsq			400	ms	Note17
Aborted sequence –bus release	Deselect_Abort			2	ms	Note18
ModSelL Setup Time	tSU_ModSelL	2			ms	Note19
ModSelL Hold Time	tHD_ModSelL			500	us	Note20

Notes:

1.Time from power-on, hot plug, or Reset release until the START condition of a READ retrieving the default register value of an arbitrary register (including a page switch).

2.Minimum pulse duration of the Reset signal to initiate a module reset.

3.Time from onset of condition or occurrence of event until associated unmasked Interrupt asserted.

4.Time from reading (clear on read) last Flag set until Interrupt deasserted, assuming that no conditions nor events causing a Flag setting are present.

5.Time from onset of Rx LOS condition to Rx LOS Flag raised and Interrupt asserted.

6.Time from Tx Failure state to Tx Failure Flag raised and Interrupt asserted.

7.Time from onset of condition or occurrence of event to associated Flag bit raised and Interrupt asserted.

8.Time from Mask bit raised while associated Flag bit is set until Interrupt deasserted.

9.Time from Mask bit ceased while associated Flag bit is set until Interrupt asserted.

10.Time from setting a OutputDisableTx<i> bit until optical output falls below 10% of nominal.For I2CMCI the time interval begins with the STOP token ending the MCI write transaction.

11.Time from clearing a OutputDisableTx<i> bit until an enabled optical output rises above 90% of nominal.For I2CMCI the time interval begins with the STOP token ending the MCI write transaction.

12.Time from the termination of the Rx Output Disable register write sequence until an enabled Rx output falls below 10% of nominal.

13.Time from the termination of the Rx Output Disable register write sequence until an enable Rx output rises above 90% of nominal.

14.This applies to Rx and Tx Auto Squelch and is the time from the termination of the register write sequence until

TITLE **800G OSFP SR8 Transceiver**	**DOC No. RFD-20240112002-002**	
	REVISION：01	**AUTHORIZED BY：Andy Yang**
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auto squelch functionality is disabled.

15.This applies to Rx and Tx Auto Squelch and is the time from the termination of the register write sequence until auto squelch functionality is enabled.

16.Time from onset of loss of Rx input signal condition until the squelched output condition is reached.

17.Time from onset of loss of Tx input signal condition until the squelched output condition is reached.

18.Delay from a host de-asserting ModSelL(at any point in a bus sequence) to the module releasing SCL and SDA.

19.ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.

20.ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.

7.Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2024/1/12	Andy Yang	Mike Sun